

11 a camera signal processing circuit for receiving an output  
12 signal of said frame memory and performing a camera process.

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1 3. (Amended) The CCD imaging apparatus of claim 2, further  
2 comprising a first reproduced signal converter being capable of outputting a  
3 reproduced signal of said recorder unit at the first and second frame rates.

1 4. (Amended) The CCD imaging apparatus of claim 3, further  
2 comprising:

3 a viewfinder for displaying an output signal of said camera signal  
4 processing circuit; and

5 a second reproduced signal converter for converting the reproduced  
6 signal from said recorder unit to the second frame rate, and for outputting the  
7 converted signal to said viewfinder.

1 5. (Amended) The CCD imaging apparatus of claim 1,

2 wherein, when the first frame rate is below a specified number, said  
3 drive pulse switching circuit generates the CCD read pulse at the first frame  
4 rate, and generates the CCD drive pulse at the second frame rate, and

5 wherein, when the first frame rate is below the specified number, said  
6 frame memory stores the output signal of said CCD after the CCD read pulse,  
7 and reads out the stored output signal of said CCD  $n/2$  times.

1 6. (Amended) The CCD imaging apparatus of claim 5, wherein  
2 the specified number is 30 frames/sec.

1 7. (Amended) The CCD imaging apparatus of claim 6, wherein  
2 the first frame rate is 24 frames/sec, 25 frames/sec, or 30 frames/sec, and  $n$  is  
3 2.

1 8. (Amended) The CCD imaging apparatus of claim 1,

2 wherein said drive pulse switching circuit includes a frame rate  
3 equalizing controller for enabling said CCD to output both a signal of the first  
4 frame rate and a signal of a third frame rate at the second frame rate, the  
5 second frame rate being a common multiple of the first and third frame rates.

1 9. (Amended) The CCD imaging apparatus of claim 8, wherein  
2 the second frame rate is 60 frames/sec or 48 frames/sec.

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1 10. (Amended) The CCD imaging apparatus of claim 9, further  
2 comprising a recorder unit for recording a signal from said camera signal  
3 processing circuit at the first and third frame rates.

1 11. (Amended) The CCD imaging apparatus of claim 10, wherein  
2 said recorder unit reproduces a signal at the second frame rate.

1 12. (Amended) The CCD imaging apparatus of claim 10, further  
2 comprising a first reproduced signal converting circuit for issuing a  
3 reproduced signal of said recorder unit at the first and second frame rates.

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1 14. (Amended) The CCD imaging apparatus of claim 1,

2 wherein said CCD is of a multiple frame interline transfer (MFIT)  
3 type for reading out a progressive scanning signal divided into odd and even  
4 fields,

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5 wherein said frame memory outputs the signal in one frame in a  
6 segment frame (SF) format by dividing the signal into odd and even fields,

7 wherein said drive pulse switching circuit comprises a read  
8 field controller for generating a CCD drive pulse to control an order of the odd  
9 and even fields being output from said CCD, and for changing the order of the  
10 odd and even fields every one frame when n is an odd number at every frame.

1           15.     (Amended) A charge coupled device (CCD) imaging  
2 apparatus comprising:

3           a CCD operable in a progressive scanning mode;

4           a drive pulse switching circuit for generating a CCD read pulse at a  
5 first frame rate, and for generating a CCD drive pulse at a second frame rate  
6 being  $n/2$  times the first frame rate,  $n$  being an integer;

7           a CCD driver for driving said CCD;

8           a camera signal processing circuit for receiving an output signal of  
9 said CCD and performing a camera process;

10          a first frame memory for storing a first signal issued from said camera  
11 signal processing circuit in one frame after the CCD read pulse, and for  
12 reading out the stored first signal at a frame rate of the first signal  $n/2$  times;  
13 and

14          a second frame memory for storing the first signal and reading out the  
15 stored first signal at the first frame rate, a reading out period of the first signal  
16 being  $n/2$  frames.

1           16.     (Amended) The CCD imaging apparatus of claim 15, wherein  
2 said second frame memory increases a number of samples in a horizontal  
3 blanking period of the first signal.

1           17.     (Amended) The CCD imaging apparatus of claim 15, further  
2 comprising a recorder unit for recording and reproducing a signal issued from  
3 said second frame memory at a rate of the signal issued from said second  
4 frame memory.

1           19.     (Amended) The CCD imaging apparatus of claim 15,  
2 wherein, when the first frame rate is below a specified number, said

3 drive pulse switching circuit generates the CCD read pulse at the first frame  
4 rate, and generates the CCD drive pulse at the second frame rate,

5 wherein, when the first frame rate is below the specified number, said  
6 first frame memory stores the first signal, and reads out the stored first signal  
7  $n/2$  times, and

8 wherein, when the first frame rate is below the specified number, said  
9 second frame memory stores the first signal, and the read out period of the  
10 first signal is  $n/2$  frames.

1 20. (Amended) The CCD imaging apparatus of claim 19, wherein  
2 the specified number is 30 frames/sec.

1 21. (Amended) The CCD imaging apparatus of claim 20, wherein  
2 the first frame rate is 24 frames/sec, 25 frames/sec, or 30 frames/sec, and  $n$  is  
3 4.

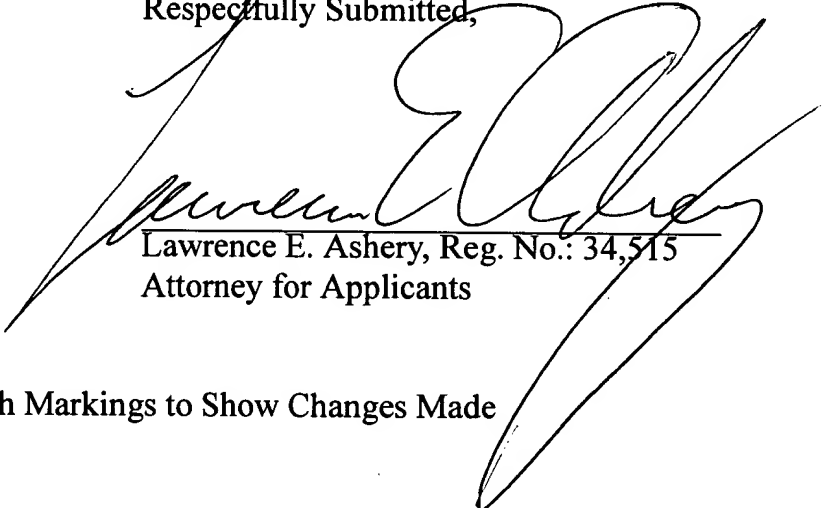
1 22. (Amended) The CCD imaging apparatus of claim 15, further  
2 comprising a first reproduced signal converter being capable of issuing a  
3 reproduced signal of said recorder unit at the first and second frame rates.

1 23. (Amended) The CCD imaging apparatus of claim 22, further  
2 comprising a second reproduced signal converter for converting a reproduced  
3 signal of said recorder unit to the second frame rate, and

4 a switching circuit for issuing outputs of said first frame memory and  
5 said second reproduced signal converter.

- 1 24. (Amended) The CCD imaging apparatus of claim 15, further  
2 comprising a power on/off circuit for turning off said camera signal processing  
3 circuit while said camera signal processing circuit does not output the first  
4 signal

Respectfully Submitted,

  
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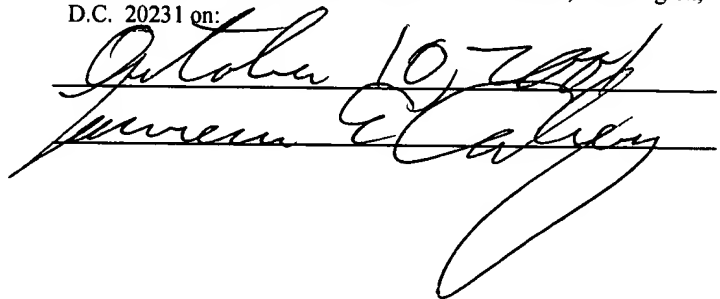
Enclosures: Version with Markings to Show Changes Made

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